In the Claims:

1-4. (Canceled)

5. (Currently Amended) ~~The method of claim 1,~~ A method of forming a semiconductor device, comprising:

forming a first interconnect level over a semiconductor substrate;

forming an uppermost interconnect level that includes an interconnect portion and a bond pad over the first interconnect level, wherein:

the interconnect portion contacts the first interconnect level by way of vias through an interlevel dielectric layer, and wherein all vias interconnecting the interconnect portion and the first interconnect level are positioned outside regions directly below the bond pad;

forming a passivation layer over the uppermost interconnect level;

removing portions of the passivation layer, wherein removing portions of the passivation layer exposes portions of the bond pad and forms a plurality of support structures overlying the uppermost surface of the bond pad; and

forming a conductive capping layer overlying the plurality of support structures, wherein the conductive capping layer electrically contacts the bond pad;

wherein the plurality of support structures are interconnected with unremoved portions of the passivation layer.

6. (Previously Presented) The method of claim 5, wherein forming the uppermost interconnect level further comprises forming the bond pad over at least one dielectric layer having a Young's modulus less than approximately 50 Giga Pascals.

7. (Canceled)

8. (Currently Amended) ~~The method of claim 1, further comprising~~ A method of forming a semiconductor device, comprising:

forming a first interconnect level over a semiconductor substrate;

forming an uppermost interconnect level that includes an interconnect portion and a bond pad over the first interconnect level, wherein:

the interconnect portion contacts the first interconnect level by way of vias through an interlevel dielectric layer, and wherein all vias interconnecting the interconnect portion and the first interconnect level are positioned outside regions directly below the bond pad;

forming a passivation layer over the uppermost interconnect level;

removing portions of the passivation layer, wherein removing portions of the passivation layer exposes portions of the bond pad and forms a plurality of support structures overlying the uppermost surface of the bond pad; and

forming a conductive capping layer overlying the plurality of support structures, wherein the conductive capping layer electrically contacts the bond pad;

forming a barrier layer between the capping layer and the bond pad, wherein the barrier layer overlies the support structures and abuts exposed portions of the bond pad.

9. (Original) The method of claim 8, wherein the barrier layer includes a material selected from a group consisting of tantalum, titanium, tungsten, and chromium.

10-27. (Canceled)

28. (Currently Amended) ~~The method of claim 24, further comprising~~ A method of forming a semiconductor device, comprising:

depositing a dielectric layer over a semiconductor substrate;

patterning and etching a trench opening within the dielectric layer;

depositing a copper layer over the dielectric layer and within the trench opening;

removing portions of the copper layer not contained within the trench opening to define an uppermost interconnect level comprising a copper bond pad and an interconnect portion, wherein the interconnect portion physically couples to an underlying interconnect level by way of vias, wherein the vias are positioned beyond regions directly below the copper bond pad;

forming a passivation layer over the uppermost copper bond pad;

patterning and etching the passivation layer to define openings and support structures overlying the uppermost copper bond pad;

depositing a conductive layer over the support structures and within the openings, wherein the conductive layer electrically contacts the uppermost copper bond pad;

patterning and etching the conductive layer to define a capping film over the support structures and the openings;

forming a barrier layer overlying the support structures and within the openings prior to forming the conductive layer, wherein the barrier layer electrically contacts the uppermost copper bond pad.

29. (Original) The method of claim 28, wherein the barrier layer is further characterized as a tantalum barrier layer.

30. (Original) The method of claim 29, wherein the conductive film is further characterized as an aluminum film.

31. (Currently Amended) The method of claim 28, wherein the barrier layer includes a material selected from a group consisting of titanium, chromium, tantalum nitride, titanium nitride, and chromium nitride[[,]].

32. (Canceled)

33. (New) The method of claim 8, wherein a copper content of uppermost interconnect level is at least 90 atomic percent.

34. (New) The method of claim 8, further comprising forming dielectric studs within the bond pad, wherein at least a portion of a support structure overlies a portion of a dielectric stud.

35. (New) The method of claim 8, wherein the dielectric layer includes a material selected from a group consisting of a nitrogen, a hydrogen, and a carbon containing silicon oxide.

36. (New) The method of claim 8, wherein the conductive capping layer includes aluminum.

37. (New) The method of claim 8, wherein the conductive capping layer includes a material selected from the group consisting of nickel and palladium.

38. (New) The method of claim 28, further comprising dielectric studs disposed within the uppermost copper bond pad, wherein at least a part of a support structure overlies a dielectric stud.

39. (New) The method of claim 28, wherein the passivation layer includes a material selected from a group consisting of nitrogen-containing silicon oxide, a hydrogen containing silicon oxide, and a carbon containing silicon oxide.

40. (New) The method of claim 28, wherein at least one of the support structures is interconnected with unremoved portions of the passivation layer.